IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

NORBERT FELBER ET AL | CH 000024

Serial No. | Group Art Unit

Filed: CONCURRENTLY | Ex.

Title: METHOD FOR TESTING INTEGRATED CIRCUITS

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

5. (amended) The method of claim 1, wherein means (14, 15; 24, 25; 34, 35) are used to electrically separate said circuit cell into the first (12; 22; 32) of said two independent cell networks and the second (13; 23; 33) of said two independent cell networks.

6. (amended) The method of claim 1, wherein load means (16, 17; 26, 27; 36, 37) are used which act as loads for said two

independent cell networks (12, 13; 22, 23; 32, 33) while at least said cell of the integrated circuit to be tested is in test mode.

8. (amended) The method of claim 4, comprising the additional step:

suppressing leakage currents in said circuit cell by turning off one or more of said control means while said circuit cell is in standby mode.

11. (amended) The integrated circuit of claim 9, comprising control circuitry (14, 15; 24, 25; 34, 35) to deactivate said p- and n-channel transistor networks (12, 13; 22, 23; 32, 33) or to electrically separate them from each other, and wherein said control circuitry is connected in series with said n- and p-channel transistor networks.

12. (amended) The integrated circuit of claim 10, further comprising load means (16, 17; 26, 27; 36, 37) which act as loads for said p- and n-channel transistor networks while said network (12, 13; 22, 23; 32, 33) is in test mode.

13. (amended) The integrated circuit of claim 10, comprising connection circuitry (38, 39) connecting electrical signals of the control circuitry (34, 35) to other subcircuits for the purpose of

testing them by selectively turning on or off said control circuitry and/or said load means (36, 37).

REMARKS

The foregoing amendments to the claims were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicants respectfully reserve all rights they may have under the Doctrine of Equivalents. Applicants furthermore reserve their right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

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APPENDIX

5. (amended) The method of claim 1~~ or 4~~, wherein means (14, 15; 24, 25; 34, 35) are used to electrically separate said circuit cell into the first (12; 22; 32) of said two independent cell networks and the second (13; 23; 33) of said two independent cell networks.

6. (amended) The method of ~~one of the claims 1 to 5~~claim 1, wherein load means (16, 17; 26, 27; 36, 37) are used which act as loads for said two independent cell networks (12, 13; 22, 23; 32, 33) while at least said cell of the integrated circuit to be tested is in test mode.

8. (amended) The method of ~~one of the claims 4 to 7~~claim 4, comprising the additional step:

suppressing leakage currents in said circuit cell by turning off one or more of said control means while said circuit cell is in standby mode.

11. (amended) The integrated circuit of claim 9~~ or 10~~, comprising control circuitry (14, 15; 24, 25; 34, 35) to deactivate said p- and n-channel transistor networks (12, 13; 22, 23; 32, 33) or to electrically separate them from each other, and wherein said

control circuitry is connected in series with said n- and p-channel transistor networks.

12. (amended) The integrated circuit of claim 10~~ or 11~~, further comprising load means (16, 17; 26, 27; 36, 37) which act as loads for said p- and n-channel transistor networks while said network (12, 13; 22, 23; 32, 33) is in test mode.

13. (amended) The integrated circuit of ~~one of the claims 10, 11, or 12~~claim 10, comprising connection circuitry (38, 39) connecting electrical signals of the control circuitry (34, 35) to other subcircuits for the purpose of testing them by selectively turning on or off said control circuitry and/or said load means (36, 37).